form, for clarity. Please enter these claims as amended. Also attached is a version with markings to show changes made to the claims.

Please amend Claims 1-5, 8, 11-18 as follows:

1. (Amended) An assembly structure for a memory device, comprising:
a substrate having at least one fold line thereon, dividing the substrate into at least two sections;
a layer of memory arrays fabricated on each of the at least two sections, each section being disposed so that the memory arrays on sections adjacent to each other form an interface in which the memory arrays are aligned to provide at least one operable electronic device with the at least two sections folded on each other along the fold line.

2. (Amended) The assembly structure recited in claim 1, wherein the fold line runs approximately down a center of a definable portion of the substrate.

3. (Amended) The assembly structure recited in claim 1, wherein at least one of the sections of memory arrays forming each interface comprises semiconductor patterns.

4. (Amended) The assembly structure recited in claim 1, wherein at least one of the sections of memory arrays forming each interface comprises conductor line patterns.

5. (Amended) The assembly structure recited in claim 1, wherein the sections forming at least one interface combine to provide a plurality of conductors and semiconductor patterns.

6. The assembly structure recited in claim 1, wherein the fold line comprises a series of aligned perforations.

7. The assembly structure recited in claim 1 wherein the fold line comprises at least one indentation in the substrate.

8. (Amended) The assembly structure recited in claim 1 wherein the fold line comprises at least one crease in the substrate.

9. The assembly structure recited in claim 1, wherein the fold line comprises a change in a property of the substrate along the fold line.

10. The assembly structure recited in claim 1, wherein there are at least two fold lines on the substrate, providing at least three sections that fold over each other to produce at least two active memory devices.

11. (Amended) The assembly structure in claim 10 wherein the three sections includes a center section having a set of conductor lines on both sides of the center section to align with memory devices on both sides of the center section after folding.

12. (Amended) An assembly structure for a memory device, comprising:
a common substrate having multiple sections;
a first layer of a memory array disposed on a first section of the multiple sections;
a second layer of a memory array disposed on a second section of the multiple sections;
at least one fold line disposed on the common substrate to define alignment of the memory arrays on the first and second sections; and
wherein the sections may be folded on each other at the fold line to form an operable electronic device in the memory device.

13. (Amended) The assembly structure of claim 12 wherein the memory array on the first section comprise a first plurality of conductor lines and the memory array on the second section comprise a second plurality of conductor lines, and wherein at least one of the memory arrays comprise semiconductor materials.

14. (Amended) The assembly structure of claim 13 wherein the memory arrays of the first and second sections are fabricated so that, with the first and second sections folded on each other at the fold line, the first and second pluralities of conductor lines and the semiconductor materials are aligned with each other to form the operable electronic device in the memory device.

15. (Amended) The assembly structure recited in claim 13, wherein the first plurality of conductor lines are formed with an array of parallel conductors spaced across the first section, and the second plurality of conductor lines are formed with an array of parallel

conductors spaced across the second section, the plurality of conductor lines on the second section being perpendicular to the plurality of conductor lines on the first section.

16. (Amended) The assembly structure recited in claim 13 wherein the first and second sections are folded along the fold line so that the layers of memory arrays are in contact with each other, and wherein at least one of the first and second sections has semiconductor materials and patterns thereon to form a matrix of memory cells.

17. (Amended) The assembly structure recited in claim 16 wherein the first plurality of conductor lines are fabricated with first narrowing cross-section areas at points where the memory cells are capable of a permanent change of state.

18. (Amended) The assembly structure recited in claim 17, wherein the second plurality of conductor lines includes second narrowing cross-section areas configured to align with the first narrowing cross-section areas.